Date of Filing: September 9, 2002
Japanese Patent Application No.: 2002-262243

[Name of Document] Application for Patent

[Reference No.] 200205449

[Date of Filing] September 9, 2002

[Addressee] Commissioner of Japan Patent Office

[Int'l Class] H04N 7/30
H04N 1/41
H03M 7/30

[Inventor]
[Address] c/o Ricoh Company, Ltd.,
3-6, Nakamagome 1-chome, Ota-ku,
Tokyo
[Name] Shogo Oneda

[Inventor]
[Address] c/o Ricoh Company, Ltd.,
3-6, Nakamagome 1-chome, Ota-ku,
Tokyo
[Name] Keiichi Suzuki

[Inventor]
[Address] c/o Ricoh Company, Ltd.,
3-6, Nakamagome 1-chome, Ota-ku,
Tokyo
[Name] Yukio Kadowaki

[Inventor]
[Address] c/o Ricoh Company, Ltd.,
3-6, Nakamagome 1-chome, Ota-ku,
Tokyo
[Name] Yutaka Sano

[Inventor]
[Address] c/o Ricoh Company, Ltd.,
3-6, Nakamagome 1-chome, Ota-ku,
Tokyo
[Name] Tooru Suino

[Inventor]

through compression and encoding of image data;

a detection means for detecting a battery remaining amount of power supply to the apparatus; and

a control means for controlling the code decompression means such that the code decompression means reduces power consumption in performing the decompression based on the detected battery remaining amount.

[Claim 2]

The image decompression apparatus according to claim 1, wherein the code decompression means comprises a code discard means for selectively discarding the code data before the decompression, and the control means causes the code discard means to selectively discard a portion of the code data to reduce the power consumption.

[Claim 3]

The image decompression apparatus according to claim 2, wherein the code decompression means divides the image data into a plurality of sub-regions, and decompresses code data produced through compression and encoding in a hierarchical manner for each of the sub-regions.

[Claim 4]

The image decompression apparatus according to claim 3, wherein the code decompression means decompresses code data produced through compression and encoding based on a JPEG 2000 algorithm.

[Claim 5]

The image decompression apparatus according to any one of claims 2 through 4, wherein the control means causes the code discard means to selectively discard a portion of the code data to decrease a frame rate of an image to reduce the power consumption.

[Claim 6]

The image decompressing apparatus according to any one of claims 2 through 5, wherein the control means causes the code discard means to selectively discard a portion of the code data to decrease resolution of an image to reduce the power consumption.

[Claim 7]

The image decompressing apparatus according to any one of claims 2 through 6, wherein the control means causes the code discard means to selectively discard a portion of the code data to decrease an image region to be displayed to reduce the power consumption.

[Claim 8]

The image decompressing apparatus according to any one of claims 2 through 7, wherein the control means reduces frequency of a clock signal used in the code decompression means to reduce the power consumption.

[Claim 9]

The image decompression apparatus according to any one of claims 1 through 8 comprising a variable voltage source for generating variable voltage from electric power supplied from the battery and supplying the variable voltage to the code decompression means, wherein the control means controls the variable voltage source to decrease the variable voltage in accordance with the reduction of power consumption.

[Claim 10]

The image decompression apparatus according to any one of claims 2 through 8 comprising a communication means for instructing a sender of the code data, instead of the code discard means, wherein the control means causes the communication means to instruct the sender to selectively discard a portion of the code data.

[Claim 11]

The image decompression apparatus according to any one of claims 2 through 8 comprising a size reading means for reading an image size, which is an image attribute, from the code data before the decompression, wherein the control means changes selective discard rate of a portion of the code data based on the read image size.

[Claim 12]

The image decompression apparatus according to any one of claims 2 through 8 comprising a acceptance means for accepting an operation

mode selected by a user from a plurality of modes for setting selective discard rate of a portion of the code data, wherein the control means changes the selective discard rate of a portion of the code data based on the received operation mode, regardless of the detected battery remaining amount.

[Name of Document] Specification

[Title of the Invention] Image Decompression Apparatus

[Technical Field]

[0001]

The present invention relates to an image decompression apparatus for decompressing code data produced through compression and encoding of image data.

[Background Art]

[0002]

A technique for suppressing power consumption by changing a thinning factor or a frame rate of image data in accordance with a battery remaining amount, and changing a clock and power source voltage of a processing circuit based on the changed values is disclosed (refer to Patent document 1).

[0003]

[Patent document 1] Japanese Patent Application Laid-Open No.2001-238189

[0004]

[Disclosure of the Invention]

[Problems to be Solved]

However, the conventional technique is for suppressing power consumption in performing compression and encoding of image data, and has no effect for suppressing power consumption in performing decompression of code data produced through compression and encoding.

[0005]

Further, with the conventional configuration, all of the code data needs to be decompressed to decompress the code data. Therefore,

to reduce the power consumption by reducing a processing amount is difficult.

[0006]

An object of the present invention is to effectively reduce the power consumption in performing processing to decompress the code data produced through compression and encoding of an image.

[0007]

[Means for Solving the Problems]

The invention of claim 1 refers to an image decompression apparatus including a code decompression means for decompressing code data produced through compression and encoding of image data, a detection means for detecting a battery remaining amount of power supply to the apparatus, and a control means for controlling the code decompression means such that the decompression means reduces power consumption in performing the decompression based on the detected battery remaining amount.

[0008]

Accordingly, the power consumption in performing processing to decompress the code data produced through compression and encoding of an image may be reduced.

[0009]

The invention of claim 2 refers to the image decompression apparatus according to claim 1, wherein the code decompression means includes a code discard means for selectively discarding the code data before the decompression, and the control means causes the code discard means to selectively discard a portion of the code data to reduce the power consumption.

[0010]

Accordingly, the power consumption may be effectively reduced by decompressing the code data after a portion of the code data is selectively discarded.

[0011]

The invention of claim 3 refers to the image decompression

apparatus according to claim 2, wherein the code decompression means divides the image data into a plurality of sub-regions, and decompresses code data produced through compression and encoding in a hierarchical manner for each of the sub-regions.

[0012]

Accordingly, the power consumption may be easily reduced as a code is easily discarded for each necessary sub-region.

[0013]

The invention of claim 4 refers to the image decompression apparatus according to claim 3, wherein the code decompression means decompresses code data produced through compression and encoding based on a JPEG 2000 algorithm.

[0014]

Accordingly, the power consumption may be easily reduced as the code is easily discarded for each necessary tile.

[0015]

The invention of claim 5 refers to the image decompression apparatus according to any one of claims 2 through 4, wherein the control means causes the code discard means to selectively discard a portion of the code data to decrease a frame rate of an image to reduce the power consumption.

[0016]

Accordingly, the power consumption may be effectively reduced by reducing the code data so as to decrease the frame rate.

[0017]

The invention of claim 6 refers to the image decompressing apparatus according to any one of claims 2 through 5, wherein the control means causes the code discard means to selectively discard a portion of the code data to decrease resolution of an image to reduce the power consumption.

[0018]

Accordingly, the power consumption may be effectively reduced by reducing the code data so as to decrease the resolution of the

image.

[0019]

The invention of claim 7 refers to the image decompressing apparatus according to any one of claims 2 through 6, wherein the control means causes the code discard means to selectively discard a portion of the code data to decrease an image region to be displayed to reduce the power consumption.

[0020]

Accordingly, the power consumption may be effectively reduced by reducing the code data so as to decrease the image region to be displayed.

[0021]

The invention of claim 8 refers to the image decompressing apparatus according to any one of claims 2 through 7, wherein the control means reduces frequency of a clock signal used in the code decompression means to reduce the power consumption.

[0022]

Accordingly, the power consumption may be effectively reduced by reducing the frequency of the clock signal.

[0023]

The invention of claim 9 refers to the image decompression apparatus according to any one of claims 1 through 8 including a variable voltage source for generating variable voltage from electric power supplied from the battery and supplying the variable voltage to the code decompression means, wherein the control means controls the variable voltage source to decrease the variable voltage in accordance with the reduction of power consumption.

[0024]

Accordingly the power consumption may be effectively reduced by decreasing the voltage used for decompressing the code data.

[0025]

The invention of claim 10 refers to the image decompression apparatus according to any one of claims 2 through 8 including a

communication means for instructing a sender of the code data, instead of the code discard means, wherein the control means causes the communication means to instruct the sender to selectively discard a portion of the code data.

[0026]

Accordingly, to selectively discard a portion of the code data to be transmitted at the sender of the code data becomes possible, and the power consumption in performing processing to discard a portion of the code data may be effectively reduced.

[0027]

The invention of claim 11 refers to the image decompression apparatus according to any one of claims 2 through 8 including a size reading means for reading an image size, which is an image attribute, from the code data before the decompression, wherein the control means changes selective discard rate of a portion of the code data based on the read image size.

[0028]

Accordingly, the power consumption may be effectively reduced regardless of the image size.

[0029]

The invention of claim 12 refers to the image decompression apparatus according to any one of claims 2 through 8 including a acceptance means for accepting an operation mode selected by a user from a plurality of modes for setting selective discard rate of a portion of the code data, wherein the control means changes the selective discard rate of a portion of the code data based on the received operation mode, regardless of the detected battery remaining amount.

[0030]

Accordingly, the user may select whether to prioritize an image, or to prioritize reduction in power consumption, as desired.

[0031]

[Best Mode for Carrying out the Invention]

An embodiment of the present invention is described.

[0032]

Fig. 1 is a block diagram showing a schematic configuration of an image decompression apparatus 1 according to an embodiment of the present invention. The image decompression apparatus 1 treats image data having been subjected to compression and encoding based on, for example, a JPEG 2000 algorithm. The image decompression apparatus 1 receives code streams of the image data from a host apparatus 12, and decompresses the code streams. The code streams are produced by dividing an image into a plurality of sub-regions (i.e., tiles) and by performing compression/encoding in a hierarchical manner for each tile, using a discrete wavelet transform (DWT).

[0033]

The image decompression apparatus 1 includes an input part 2, code discard part, entropy decoder, dequantization part, inverse discrete wavelet transform (DWT) part 6, and clock generation part 9, to form a code decompression means. The image decompression apparatus includes the input part 2 for receiving an input of code streams from the host apparatus 12, code discard part 3 for selectively discarding a portion of codes contained in the received code stream, with reference to header data or the like, entropy decoder 4 for performing entropy decoding of the data after the code discard process, dequantization part 5 for dequantizing the entropy-decoded data, and inverse DWT part 6 for carrying out inverse discrete wavelet transform (DWT) on the dequantized data, and outputting the decompressed image data.

[0034]

A battery 7 is a power supply of the image decompression apparatus 1. A variable voltage source 8 generates a variable voltage from the power supplied from the battery 7, and supplies the variable voltage to the input part 2, code discard part 3, entropy decoder 4, dequantization part 5, and inverse DWT part 6. Although the image

decompression apparatus 1 uses the battery 7 as the power supply, an AC power source may be used to drive the image decompression apparatus 1. The clock generation part 9 generates and supplies clock signals to the code discard part 3, entropy decoder 4, dequantization part 5, and inverse DWT part 6. A control part 10 includes, a microcomputer, etc., and controls an entire operation of the image decompression apparatus 1. The power source state detection part 11 detects a remaining amount of the battery 7 using a known technique.

[0035]

The image decompression apparatus 1 is used in image display apparatuses such a camera monitoring system, or the like. When the image decompression apparatus is applied to the camera monitoring system, image data decompressed by the image decompression apparatus 1 is buffered in a storage medium such as a hard disk, and the decompressed images are displayed on a monitor screen.

[0036]

Fig. 2 is a flow chart showing processing performed by the control part 10. The control part 10 detects a battery remaining amount of the power source state detection part 11 (step S1), and compares the detection result with one or more predetermined threshold values (step S2). When using two or more threshold values, the threshold values are set to multiple levels such as 3/4, 2/4, and 1/4 of a full charge battery state. To realize a control means, the control part 10 controls associated parts such as the input part 2, code discard part 3, entropy decoder 4, dequantization part 5, inverse DWT part 6, and clock generation part 9 based on the comparison result of step S2 (step S3) to reduce power consumption of the image decompression apparatus 1.

[0037]

That is, in step S3, the code discard part 3 selectively discards unnecessary portions of the code streams received at the input part 2. At the same time, a mode of the entropy decoder 4 is changed

to decrease the amount of codes to be subjected to entropy decoding. The mode change includes change in the frame rate of the image and/or the amount of decoded data for each frame (resolution, image quality, and displayed regions). In response to the reduction of the data amount to be processed by the entropy decoder 4 through the mode change, the control part 10 controls the power source voltages of the entropy decoder 4, dequantization unit 5 and inverse DWT unit 6, and the frequency of the clock signals generated by the clock generation part 9, to reduce power consumption in each part. Accordingly, the control part 10 also controls the variable voltage source 8 in order to decrease the output voltage level.

[0038]

An example of mode changes is explained in detail below.

[0039]

Fig. 3 is an explanatory diagram showing processing for reducing an amount of codes to be entropy decoded by controlling frame rate. In such a case, the frame rate is reduced to a half, and every one of two adjacent frames is reproduced. Consequently, workload of the entropy decoder 4, dequantization part 5, and inverse DWT part 6 becomes 1/2, and frequency of clock signals generated by the clock generation part 9 is reduced to a half. Therefore, the variable voltage output from the variable voltage source 8 may be reduced. As a result, power consumption may be greatly reduced.

[0040]

Fig. 4 is an explanatory diagram showing processing for decreasing resolution of an image by reducing an amount of codes that are to be subjected to entropy decoding. The code amount is reduced by discarding a portion of a plurality of subbands for configuring each frame. The code data is input to the code discard part 3 in an each subband code (4 to 0 are each subband code order), as shown in Fig. 4. A boundary mark is inserted between two adjacent subbands. The code discard part 3 recognizes boundaries of the subbands by detecting the boundary marks, and may selectively

discard subbands. The subbands are subjected to entropy decoding starting from subband 4 (no significant meaning in symbol "4"). If the remaining amount of the battery 7 is sufficient, entropy decoding is processed up to the last subband "0". If the remaining amount of the battery 7 is insufficient, entropy decoding is processed up to subband 1, or subband 2 or 3, and rest of the subbands may be discarded. Therefore, the variable voltage output from the variable voltage source 8 may be reduced. As a result, power consumption may be greatly reduced.

[0041]

Fig. 5 shows a data structure of a subband shown in Fig. 4. In the subband, data encoded in an order from the most significant bit (MSB) of the bit plane is stored. The code amount may be reduced not by discarding an entire single subband, but by carrying out entropy decoding from the MSB toward the LSB so as to discard the last two bit planes. In such a case, an amount of code data processed by the entropy decoder 4 may also be reduced. However, an amount of data processed by the dequantization part 5 and the inverse DWT part 6 may be unchanged.

[0042]

The operations explained above are also applicable to non-tiled encoded data.

[0043]

Fig. 6 is an explanatory diagram showing an example of decreasing an image area to be displayed by carrying out entropy decoding for only a center region of an image to reduce the image area to be displayed in order to reduce a code amount. In the example, for each of three color components R, G, and B, only a predetermined area of the center region of the image (four center tiles in the example shown in Fig. 6) is subjected to entropy decoding, and the rest of the tiles are discarded.

[0044]

Another example of mode changes includes change in the image

quality. For example, regarding a color image, only luminance signals may be subjected to entropy decoding, and color difference signals may be discarded. In such a case, a monochrome image is displayed.

[0045]

In Fig. 1, the code discard part 3 selectively discards codes. However, as shown in Fig. 7, to realize a communication means, the control part 10 may cause a communication part 13 having a predetermined communication interface to notify the host apparatus 12 of the code data that are to be discarded, and to instruct discarding of the code. The host apparatus 12 creates code streams in which predetermined codes are discarded in advance, and sends to the image decompression apparatus 1. In such a case, the image decompression apparatus 1 is not required to include the code discard part 3. Accordingly, the code discard part 3 become unnecessary, and a processing amount of codes at the input part 2 may be reduced. As a result, the power consumption may be more effectively reduced.

[0046]

Table 1 shows correspondence relation between a power source state, and control of frame rate, resolution and display region, clock frequency setting and power source voltage of the variable voltage source 8. In the column of "power source state", "AC" denotes that an AC power source is used, and "Full" through "1/4 Max." denote remaining amount of the battery. "Full" denotes that the remaining amount of the battery is greater than 3/4 of the 100% state battery. "3/4 MAX." denotes that the remaining amount of the battery is equal to or less than 3/4 of the full state. The same applies to "2/4 MAX." and "1/4 MAX.". In the example, the current state of the power supply is determined in a hierarchical manner using the threshold values (step S2) described above. For each level of the power supply state, corresponding parameters are defined for the frame rate, resolution, display region, clock frequency, and power source

voltage of the variable voltage source 8.

[0047]

The control part 10 stores each setting value of the frame rate, resolution, display region, clock frequency and power source voltage corresponding to the power source state like as shown in Table 1 as table data, determines a current power source state based on step S2, and sets each setting value of the resolution, display region, clock frequency and power source voltage corresponding to the power source state that is registered in the table data. Therefore, power source voltage values shown in Table 1 may be output from the variable voltage source 8. As a result, the power consumption may be reduced.

[0048]

[Table 1]

Power Source State	Frame Rate	Resolution	Display Region	Clock Setting	Power Source Voltage
AC	Full	Full	Whole	1/1 Clock	3.3V
Full	1/2	Full	Whole	1/2 Clock	3.1V
3/4 MAX.	1/2	1/2	Whole	1/4 Clock	2.9V
2/4 MAX.	1/4	1/2	Whole	1/8 Clock	2.7V
1/4 MAX.	1/4	1/4	Center Area	1/16 Clock	2.5V

[0049]

If the frame rate is reduced from full frame to 1/2 frame, the processing amount of codes becomes a half, the clock frequency may be reduced to 1/2, and the power source voltage may be reduced. If the resolution is reduced to 1/2, subband "0" shown in Fig. 4 is discarded for each frame, and the amount of code data to be processed for each frame is reduced to 1/2, the data processing amount in the dequantization part 5 and the inverse DWT part 6 is reduced to 1/2, and the clock frequency may be set to 1/2 (total 1/4).

[0050]

The data processing amount depends on the circuit configuration, and may not be reduced exactly to 1/2. Accordingly, the actual clock frequency may be reduced as much as possible according to the circuit configuration. Similarly, since the code amount depends on the contents of the image data, the code amount may not be reduced exactly to 1/2. Accordingly, even if the clock frequency is controlled precisely in accordance with the data processing amounts in each part of the entropy decoder 4, decoding processing may not be performed sufficiently. In such a case, the decoding results are all treated as "0", or "1". As has been explained referring to Figs. 4 and 5, decoding is carried out, giving priority to more important code data. Accordingly, even if code data not being subjected to the decoding processing are omitted, only lower bit plane data or lower-level subband data are missed, which may cause deterioration of the tone or the resolution, but may not lead to significant deterioration of image quality.

[0051]

Processing shown in Fig. 8 may be performed instead of the processing shown in Fig. 2. Steps S1 through S3 in the processing shown in Fig. 8 is similar to a case of Fig. 2. In step S4, an image size recorded as an image attribute in a main header and a frame header of code streams is read by the code discard part 3 to realize a size reading means.

[0052]

Assuming that Table 1 is an example of the frame rate, resolution, display region, clock frequency and power source voltage of the variable voltage source 8 when an image size is small, Table 2 is a similar example of a case when an image size is large. When the image size is large, original image data contains more high-frequency components. Accordingly, even if the resolution is reduced, the image quality is not adversely affected, and the setting may be changed from the setting shown in Table 1 to the setting shown in Table 2.

[0053]

[Table 2]

Power Source State	Frame Rate	Resolution	Display Region	Clock Setting	Power Source Voltage
AC	Full	Full	Whole	1/1 Clock	3.3V
Full	Full	1/2	Whole	1/2 Clock	3.1V
3/4 MAX.	1/2	1/2	Whole	1/4 Clock	2.9V
2/4 MAX.	1/2	1/4	Whole	1/8 Clock	2.7V
1/4 MAX.	1/4	1/4	Center Area	1/16 Clock	2.5V

[0054]

That is, to realize the control means, each setting value of the frame rate, resolution, display region, clock frequency and power source voltage corresponding to power source states like as shown in Table 1 is stored as first table data, similar data like as shown in Table 2 is stored as second table data, the control part 10 selects one of the above table data (step S5) based on the determination of step S4, and the selected table data is used for the processing in step S3. Accordingly, selective discard rate of a portion of the code data may be changed depending on the image size. As a result, the power source voltage may be effectively decreased regardless of the image size.

[0055]

The image decompression apparatus 1 may include an operation mode setting part 14, as shown in Fig. 9. The operation mode setting part 14 accepts an operation mode input from a user through an operation of a predetermined operation panel. The operation mode is, for example, power saving modes 1 through 4 shown in Table 3. Each setting value of resolution, display region, clock frequency, and power source voltage is set for the power saving modes 1 through 4, similar to cases of Tables 1 and 2. The control part 10 includes table data like as Table 3. The power source voltage is set to become smaller in an order of the power saving modes 1 to 4. As a result,

the power consumption may be more effectively reduced.

[0056]

[Table 3]

Power Source State	Frame Rate	Resolution	Display Region	Clock Setting	Power Source Voltage
Power Saving Mode 1	1/2	Full	Whole	1/2 Clock	3.1V
Power Saving Mode 2	1/2	1/2	Whole	1/4 Clock	2.9V
Power Saving Mode 3	1/4	1/2	Whole	1/8 Clock	2.7V
Power Saving Mode 4	1/4	1/4	Whole	1/16 Clock	2.5V

[0057]

In such a case, processing like as shown in Fig. 10 is performed. That is, the control part 10 accepts an operation mode input from a user by the operation mode setting part 14 (step S6: Y) to realize a acceptance means, prohibits to perform processing of Fig. 2, or 8 (step S7) to realize a control means, and sets one of each setting value of the resolution, display region, clock frequency and power source voltage from the power saving modes 1 through 4 being input in step S6 based on the table data like as Table 3 (step S8). The setting is forcedly performed by step S7, regardless of the setting processed in steps S1 through S5. Accordingly, the user may set selective discard rate of a portion of the code data, as desired, by selecting the power saving modes 1 through 4, regardless of the remaining amount of the battery 7. The user may select any one of the power saving modes 1 through 4 considering whether to desire a high quality image even the power consumption is large, or to desire reduction in power consumption even image quality is bad.

[0058]

[Effect of the Invention]

The invention of claim 1 may effectively reduce power consumption in performing processing to decompress code data produced through compression and encoding of an image.

[0059]

The invention of claim 2 according to the invention of claim 1 may effectively reduce power consumption by decompressing the code data after a portion of the code data is selectively discarded.

[0060]

The invention of claim 3 according to the invention of claim 2 may easily reduce power consumption as the code may be easily discarded for each necessary sub-region.

[0061]

The invention of claim 4 according to the invention of claim 3 may easily reduce power consumption as the code may be discarded for each tile.

[0062]

The invention of claim 5 according to the invention described in any one of claims 2 through 4 may effectively reduce power consumption by reducing the code data so as to decrease a frame rate.

[0063]

The invention of claim 6 according to the invention described in any one of claims 2 through 5 may effectively reduce power consumption by reducing the code data so as to decrease resolution.

[0064]

The invention of claim 7 according to the invention described in any one of claims 2 through 6 may effectively reduce power consumption by reducing the code data so as to decrease an image region to be displayed.

[0065]

The invention of claim 8 according to the invention described in any one of claims 2 through 7 may effectively reduce power consumption by reducing frequency of a clock signal.

[0066]

The invention of claim 9 according to the invention described in any one of claims 1 through 8 may effectively reduce power consumption by decreasing voltage used for decompressing the code

data.

[0067]

The invention of claim 10 according to the invention described in any one of claims 2 through 8 may perform selective discard of a portion of the code data to be sent at a sender of the code data. Accordingly, power consumption in performing processing to discard a portion of the code data may be effectively reduced.

[0068]

The invention of claim 11 according to the invention described in any one of claims 2 through 8 may effectively reduce power consumption regardless of an image size.

[0069]

The invention of claim 12 according to the invention described in any one of claims 2 through 8, wherein a user may select whether to prioritize a reduction in power consumption, or to prioritize an image.

[Brief Description of the Drawings]

[Fig. 1]

Fig. 1 is a block diagram for explaining a configuration of an image decompression apparatus according to an embodiment of the present invention.

[Fig. 2]

Fig. 2 is a flowchart of processing performed by the image decompression apparatus.

[Fig. 3]

Fig. 3 is an explanatory diagram of processing for changing frame rate.

[Fig. 4]

Fig. 4 is an explanatory diagram of processing for changing resolution.

[Fig. 5]

Fig. 5 is an explanatory diagram of processing for changing resolution.

[Fig. 6]

Fig. 6 is an explanatory diagram of processing for changing an image region to be displayed.

[Fig. 7]

Fig. 7 is a block diagram for explaining a configuration of another image decompression apparatus.

[Fig. 8]

Fig. 8 is a flowchart of another processing example performed by the image decompression apparatus.

[Fig. 9]

Fig. 9 is a block diagram for explaining a configuration of another image decompression apparatus.

[Fig. 10]

Fig. 10 is a flowchart of another processing example performed by the image decompression apparatus.

[Reference Numerals]

1	Image decompression apparatus
2~6, 9	Image decompression means
7	Battery
8	Variable voltage source
12	Address
13	Communication means

[Name of Document] Abstract of the Disclosure

[Abstract]

[Objectives of the Invention]

To effectively reduce power consumption in performing processing to decompress code data produced through compression and encoding of an image.

[Means for Achieving the Objectives]

A power source state detection part 11 detects a remaining amount of a battery 7. A control part 10 causes a code discard part 3 to selectively discard codes of code streams so as to decrease a frame rate or resolution, or reduce image regions to be displayed, when

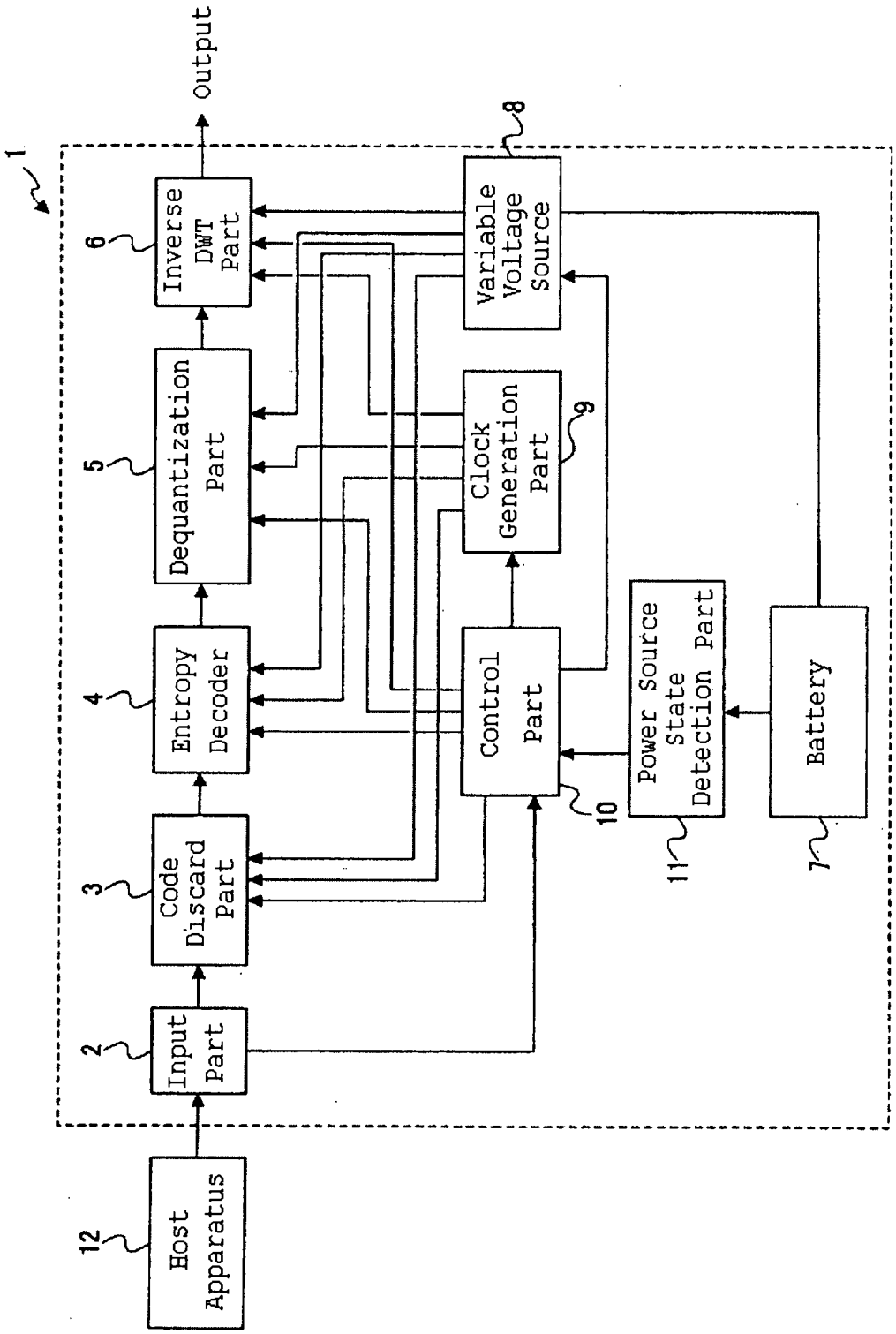
the remaining amount of the battery is low. In addition, the control part 10 causes a clock generation part 9 to reduce frequency of clock signals, and a variable voltage source 8 to decrease output voltage.

[Selected Drawing]

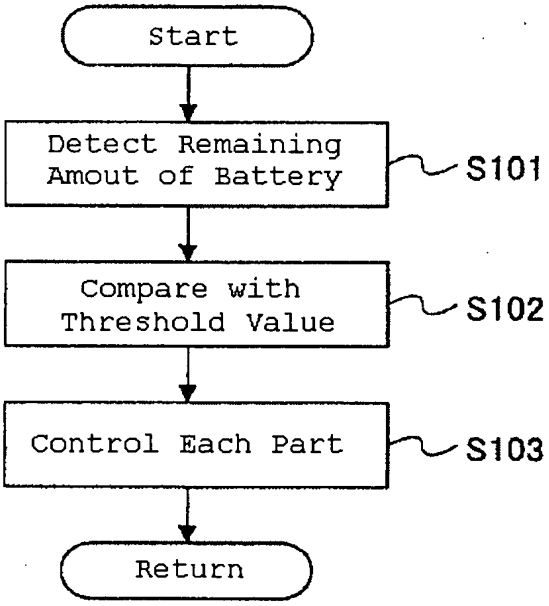
Fig. 1

[Name of Document]

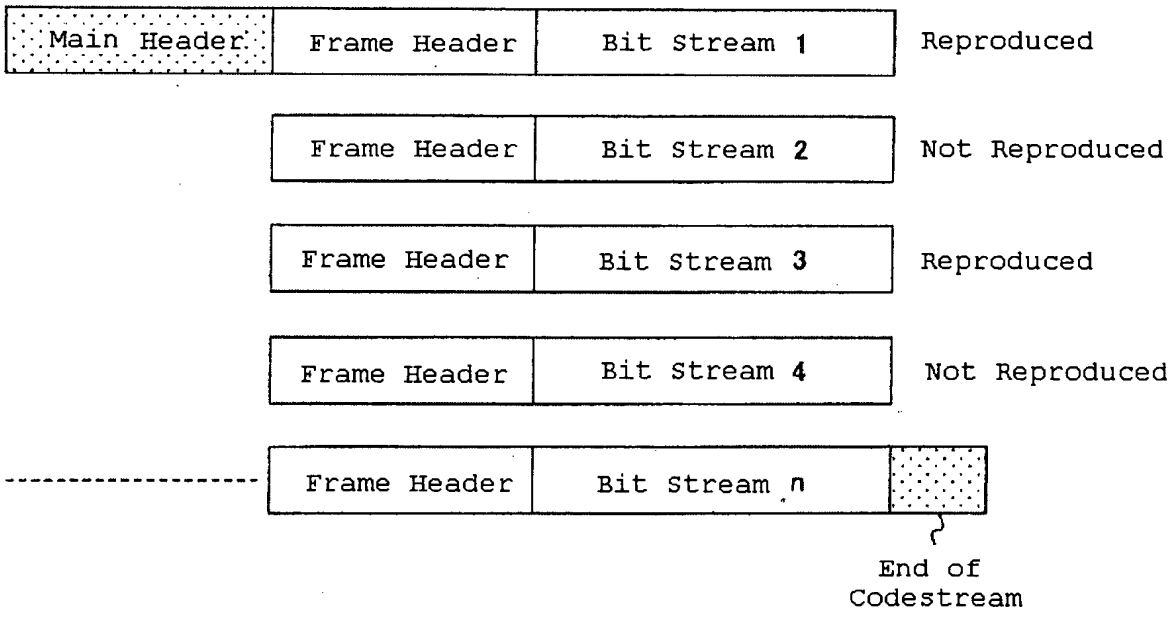
[Fig. 1]



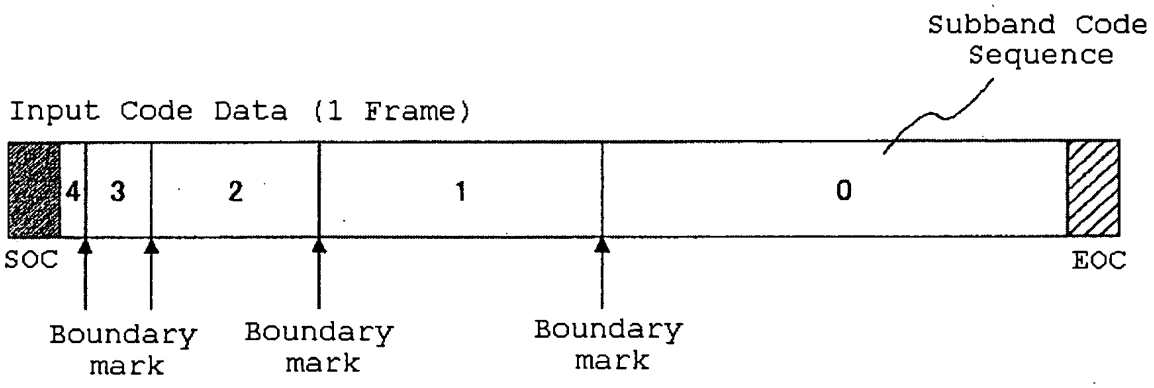
[Fig. 2]


Start
Detect Remaining Amout of Battery
S101
Compare with Threshold Value
S102
Control Each Part
S103
Return

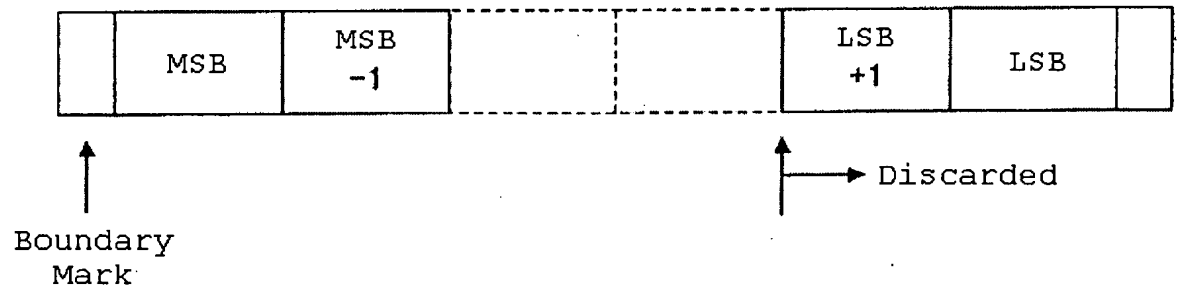
[Fig. 3]


Main Header
Frame Header
Bit Stream 1
Reproduced
Frame Header
Bit Stream 2
Not Reproduced
Frame Header
Bit Stream 3
Reproduced
Frame Header
Bit Stream 4
Not Reproduced
Frame Header
Bit Stream n
End of Codestream

[Fig. 4]

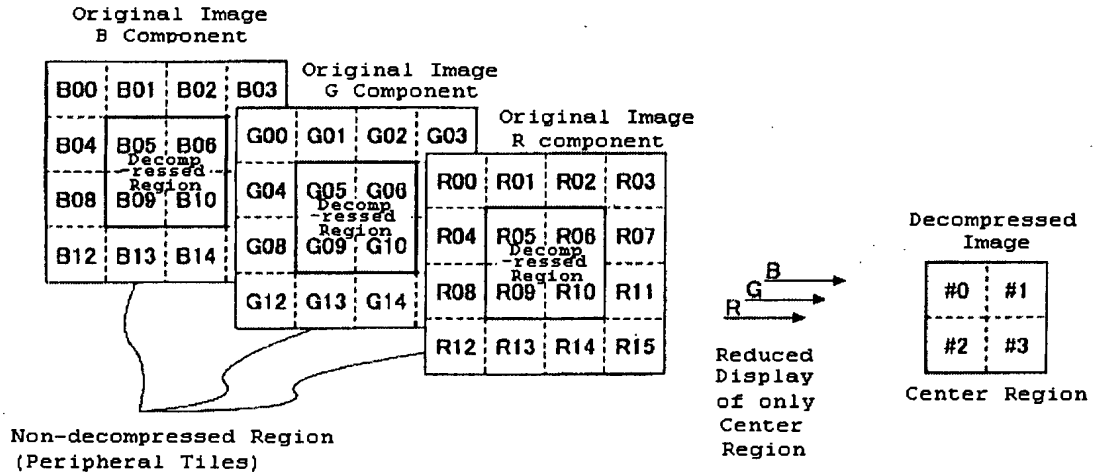


[Fig. 5]

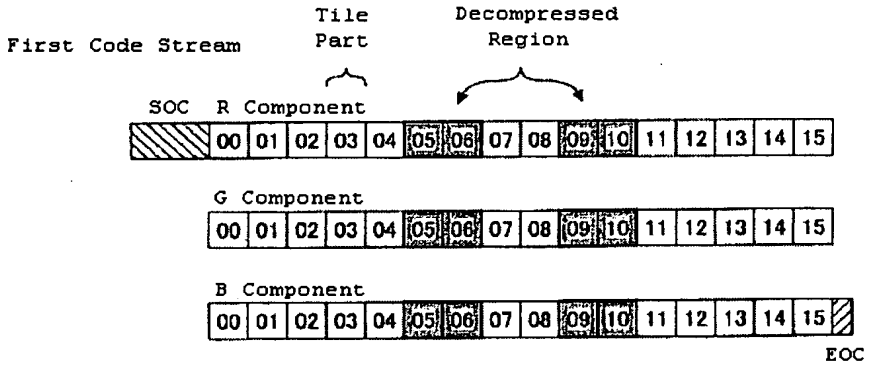


[Fig. 6]

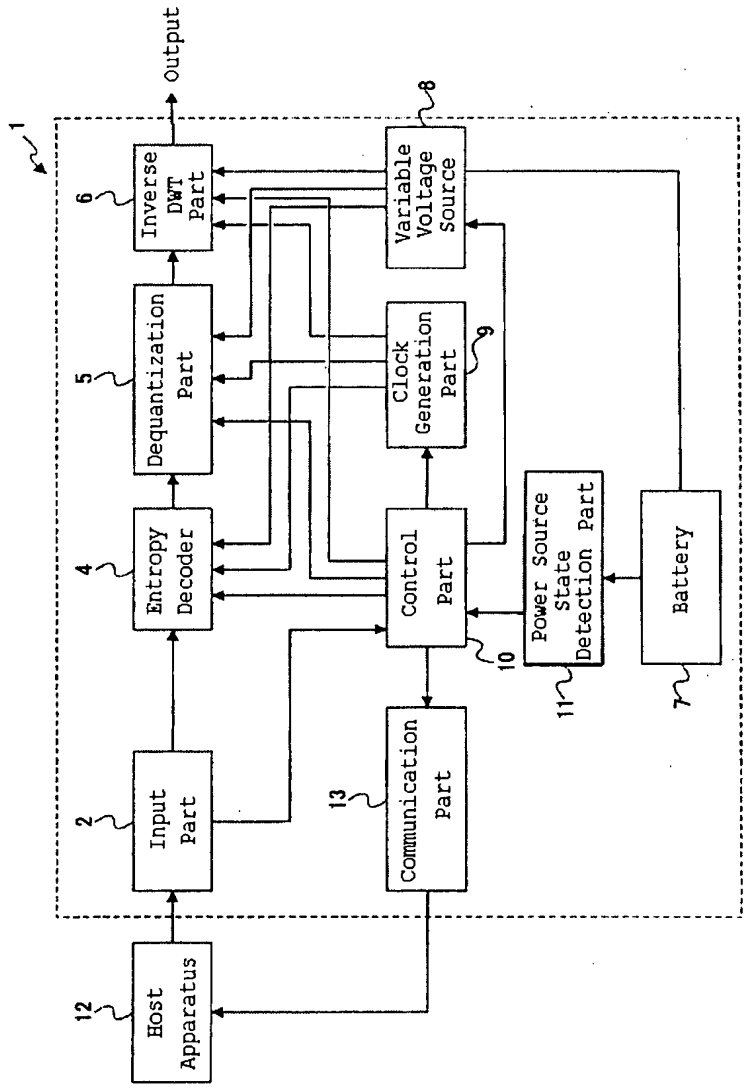
(a)



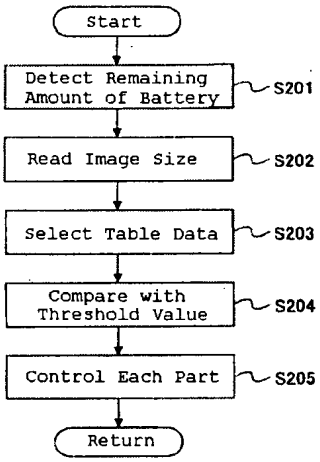
(b)


First Code Stream
Tile Part
Decompressed Region
SOC
R Component
G Component
B Component
00 01 02 03 04 05 06 07 08 09 10 11 12 13 14 15
EOC

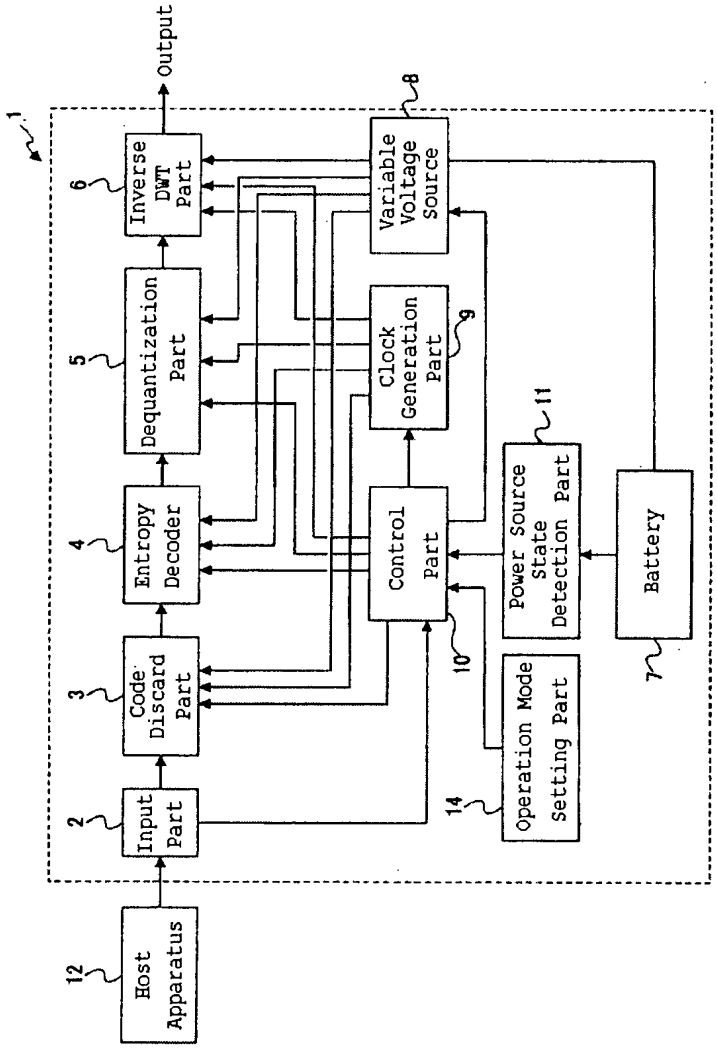
[Fig. 7]


Output
1
Inverse DWT Part
6
Dequantization Part
5
Entropy Decoder
4
Input Part
2
Host Apparatus
12
Variable Voltage Source
8
Clock Generation Part
9
Control Part
10
Power Source State Detection Part
11
Battery
7
Communication Part
13

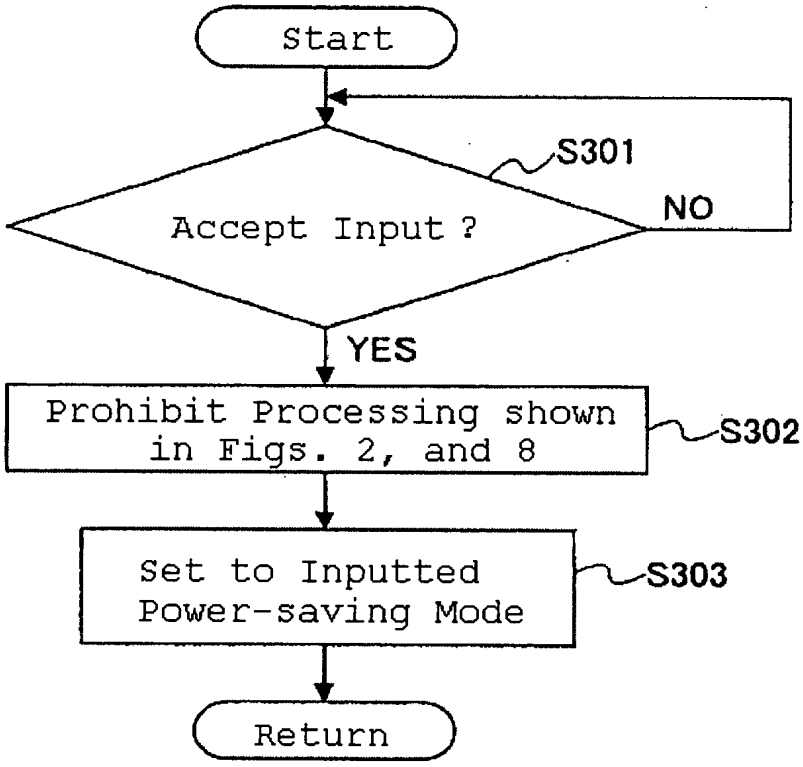
[Fig. 8]


Start
Detect Remaining Amount of Battery
S201
Read Image Size
S202
Select Table Data
S203
Compare with Threshold Value
S204
Control Each Part
S205
Return

[Fig. 9]


Output
1
Inverse DWT Part
6
Dequantization Part
5
Entropy Decoder
4
Code Discard Part
3
Input Part
2
Host Apparatus
12
Variable Voltage Source
8
Clock Generation Part
9
Control Part
10
Power Source State Detection Part
11
Battery
7
Operation Mode Setting Part
14

[Fig. 10]


Start
S301
Accept Input ?
NO
YES
Prohibit Processing shown in Figs. 2, and 8
S302
Set to Inputted Power-saving Mode
S303
Return